# XC6101 ~ XC6107, XC6111 ~ XC6117 Series

TOREX

## *Voltage Detector (VDF=1.6V~5.0V)*

***Preliminary***

- ◆CMOS Voltage Detector
- ◆Manual Reset Input
- ◆Watchdog Functions
- ◆Built-in Delay Circuit
- ◆Detect Voltage Range: 1.6~5.0V, ± 2%
- ◆Reset Function is Selectable
  VDFL (Low When Detected)
  VDFH (High When Detected)

## ■APPLICATIONS

- ●Microprocessor reset circuits
- ●Memory battery backup circuits
- ●System power-on reset circuits
- ●Power failure detection

## ■GENERAL DESCRIPTION

The XC6101~XC6107, XC6111~XC6117 series are groups of high-precision, low current consumption voltage detectors with manual reset input function and watchdog functions incorporating CMOS process technology. The series consist of a reference voltage source, delay circuit, comparator, and output driver.

With the built-in delay circuit, the XC6101 ~ XC6107, XC6111 ~ XC6117 series' ICs do not require any external components to output signals with release delay time. Moreover, with the manual reset function, reset can be asserted at any time. The ICs produce two types of output; VDFL (low when detected) and VDFH (high when detected).

With the XC6101 ~ XC6105, XC6111 ~ XC6115 series' ICs, the WD pin can be left open if the watchdog function is not used.

Whenever the watchdog pin is opened, the internal counter clears before the watchdog timeout occurs. Since the manual reset pin is internally pulled up to the VIN pin voltage level, the ICs can be used with the manual reset pin left unconnected if the pin is unused.

The detect voltages are internally fixed 1.6V ~ 5.0V in increments of 100mV, using laser trimming technology.

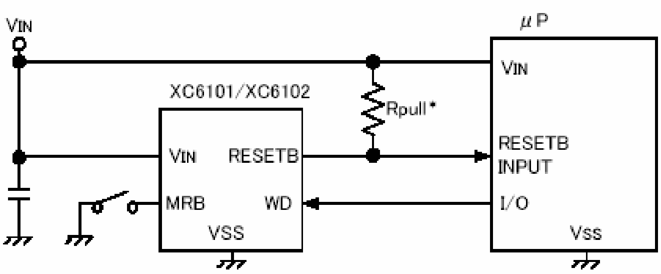
Six watchdog timeout period settings are available in a range from 6.25msec to 1.6sec.

Seven release delay time 1 are available in a range from 3.13msec to 1.6sec.

## ■FEATURES

| | |
|---|---|
| **Detect Voltage Range** | : 1.6V ~ 5.0V, ±2% (100mV increments) |
| **Hysteresis Range** | : VDF x 5%, TYP. (XC6101~XC6107)<br>VDF x 0.1%, TYP. (XC6111~XC6117) |
| **Operating Voltage Range** | : 1.0V ~ 6.0V |
| **Detect Voltage Temperature Characteristics** | : ±100ppm/°C (TYP.) |
| **Output Configuration** | : N-channel open drain, CMOS |
| **Watchdog Pin** | : Watchdog input<br>If watchdog input maintains 'H' or 'L' within the watchdog timeout period, a reset signal is output to the RESET output pin |
| **Manual Reset Pin** | : When driven 'H' to 'L' level signal, the MRB pin voltage asserts forced reset on the output pin. |
| **Release Delay Time** | : 1.6sec, 400msec, 200msec, 100msec, 50msec, 25msec, 3.13msec (TYP.) can be selectable. |
| **Watchdog Timeout Period** | : 1.6sec, 400msec, 200msec, 100msec, 50msec, 6.25msec (TYP.) can be selectable. |

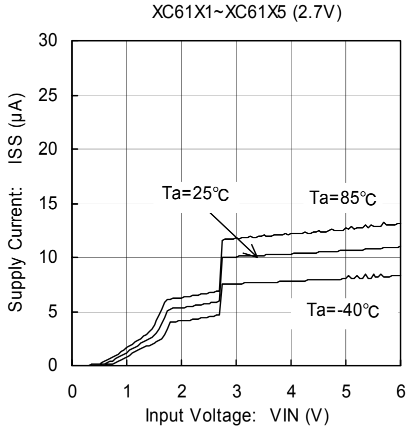
## ■TYPICAL APPLICATION CIRCUIT




* Not necessary with CMOS output products.

## ■TYPICAL PERFORMANCE CHARACTERISTICS

●Supply Current vs. Input Voltage

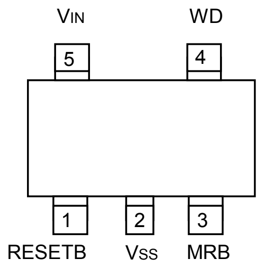



* 'x' represents both '0' and '1'. (ex. XC61x1⇒XC6101 and XC6111)

## ■PIN CONFIGURATION

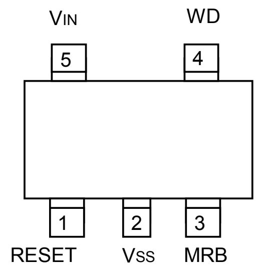
●SOT-25

XC6101, XC6102 Series
XC6111, XC6112 Series



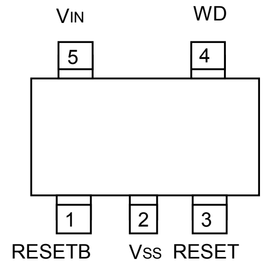

SOT-25 (TOP VIEW)

XC6103 & XC6113 Series



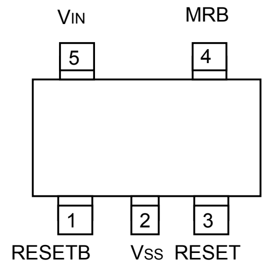

SOT-25 (TOP VIEW)

XC6104, XC6105 Series
XC6114, XC6115 Series




SOT-25 (TOP VIEW)

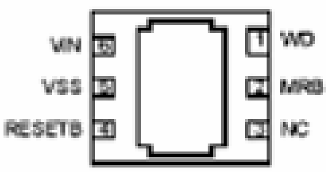
XC6106, XC6107 Series
XC6116, XC6117 Series




SOT-25 (TOP VIEW)

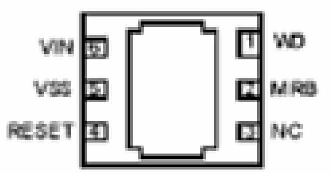
●USP-6C

XC6101, XC6102 Series
XC6111, XC6112 Series



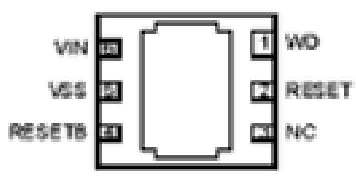

USP-6C (BOTTOM VIEW)

XC6103 & XC6113 Series



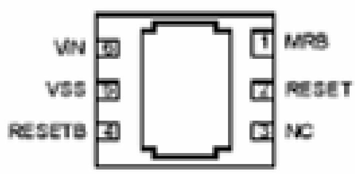

USP-6C (BOTTOM VIEW)

XC6104, XC6105 Series
XC6114, XC6115 Series




USP-6C (BOTTOM VIEW)

XC6106, XC6107 Series
XC6116, XC6117 Series




USP-6C (BOTTOM VIEW)

* The dissipation pad for the USP-6C package should be solder-plated in recommended mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the VSS pin.

## ■PIN ASSIGNMENT

| PIN NUMBER | | | | | | | | PIN NAME | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|
| XC6101, XC6102 | | XC6103 | | XC6104, XC6105 | | XC6106, XC6107 | | | |
| XC6111, XC6112 | | XC6113 | | XC6114, XC6115 | | XC6116, XC6117 | | | |
| SOT-25 | USP-6C | SOT-25 | USP-6C | SOT-25 | USP-6C | SOT-25 | USP-6C | | |
| 1 | 4 | - | - | 1 | 4 | 1 | 4 | RESETB | Reset Output (VDFL: Low Level When Detected) |
| 2 | 5 | 2 | 5 | 2 | 5 | 2 | 5 | VSS | Ground |
| 3 | 2 | 3 | 2 | - | - | 4 | 1 | MRB | Manual Reset |
| 4 | 1 | 4 | 1 | 4 | 1 | - | - | WD | Watchdog |
| 5 | 6 | 5 | 6 | 5 | 6 | 5 | 6 | VIN | Power Input |
| - | - | 1 | 4 | 3 | 2 | 3 | 2 | RESET | Reset Output (VDFH: High Level When Detected) |

# ■PRODUCT CLASSIFICATION

●Selection Guide

| SERIES | | WATCHDOG | MANUAL RESET | RESET OUTPUT | |
|---|---|---|---|---|---|
| | | | | $V_{DFL}$ (RESETB) | $V_{DFH}$ (RESET) |
| XC6101 | XC6111 | Available | Available | CMOS | - |
| XC6102 | XC6112 | Available | Available | N-channel open drain | - |
| XC6103 | XC6113 | Available | Available | - | CMOS |
| XC6104 | XC6114 | Available | Not Available | CMOS | CMOS |
| XC6105 | XC6115 | Available | Not Available | N-channel open drain | CMOS |
| XC6106 | XC6116 | Not Available | Available | CMOS | CMOS |
| XC6107 | XC6117 | Not Available | Available | N-channel open drain | CMOS |

●Ordering Information

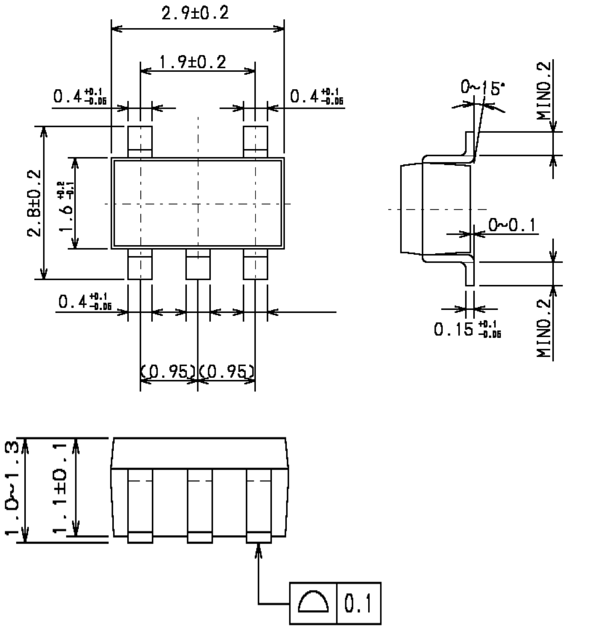
XC61①②③④⑤⑥⑦⑧

| DESIGNATOR | DESCRIPTION | SYMBOL | DESCRIPTION |
|---|---|---|---|
| ① | Hysteresis Range | 0 | : $V_{DF}$ x 5% (TYP.) with hysteresis |
| | | 1 | : $V_{DF}$ x 0.1% (TYP.) without hysteresis |
| ② | Functions and Type of Reset Output | 1 ~ 7 | : Watchdog and manual functions, and reset output type as per Selection Guide in the above chart |
| ③ | Release Delay Time * | A | : 3.13msec (TYP.) |
| | | B | : 25msec (TYP.) |
| | | C | : 50msec (TYP.) |
| | | D | : 100msec (TYP.) |
| | | E | : 200msec (TYP.) |
| | | F | : 400msec (TYP.) |
| | | H | : 1.6sec (TYP.) |
| ④ | Watchdog Timeout Period | 0 | : No WD timeout period for XC6106, XC6107, XC6116, XC6117 Series |
| | | 1 | : 6.25msec (TYP.) |
| | | 2 | : 50msec (TYP.) |
| | | 3 | : 100msec (TYP.) |
| | | 4 | : 200msec (TYP.) |
| | | 5 | : 400msec (TYP.) |
| | | 6 | : 1.6sec (TYP.) |
| ⑤⑥ | Detect Voltage | 16 ~ 50 | : Detect voltage ex.) 4.5V: ⑤⇒4, ⑥⇒5 |
| ⑦ | Package | M | : SOT-25 |
| | | E | : USP-6C |
| ⑧ | Device Orientation | R | : Embossed tape, standard feed |
| | | L | : Embossed tape, reverse feed |

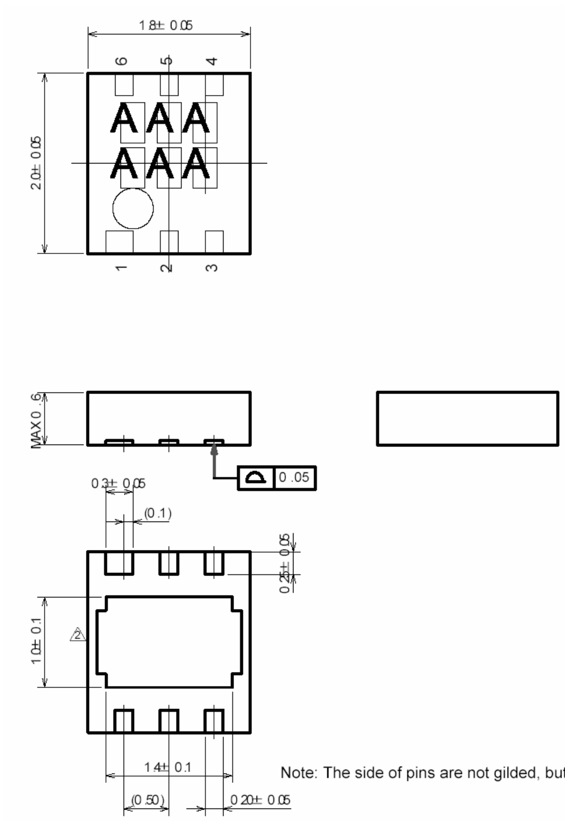
* Please set the release delay time shorter than or equal to the watchdog timeout period.
ex.) XC6101D427MR or XC6101D327MR

## ■PACKAGING INFORMATION

●SOT-25



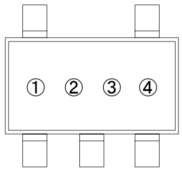

●USP-6C




Note: The side of pins are not gilded, but nickel is used.

# ■MARKING RULE

●SOT-25




SOT-25
(TOP VIEW)

① Represents product series

| MARK | PRODUCT SERIES | MARK | PRODUCT SERIES |
|---|---|---|---|
| 0 | XC6101xxxxxx | 7 | XC6111xxxxxx |
| 1 | XC6102xxxxxx | 8 | XC6112xxxxxx |
| 2 | XC6103xxxxxx | 9 | XC6113xxxxxx |
| 3 | XC6104xxxxxx | A | XC6114xxxxxx |
| 4 | XC6105xxxxxx | B | XC6115xxxxxx |
| 5 | XC6106xxxxxx | C | XC6116xxxxxx |
| 6 | XC6107xxxxxx | D | XC6117xxxxxx |

② Represents release delay time and watchdog timeout period

| MARK | RELEASE DELAY TIME | WATCH DOG TIMEOUT PERIOD | PRODUCT SERIES | MARK | RELEASE DELAY TIME | WATCH DOG TIMEOUT PERIOD | PRODUCT SERIES |
|---|---|---|---|---|---|---|---|
| A | 3.13msec | XC61X6, XC61X7 series | XC61xxA0xxxx | E | 50msec | 400msec | XC61xxC5xxxx |
| 0 | 3.13msec | 6.25msec | XC61xxA1xxxx | F | 50msec | 1.6sec | XC61xxC6xxxx |
| 1 | 3.13msec | 50msec | XC61xxA2xxxx | D | 100msec | XC61X6, XC61X7 series | XC61xxD0xxxx |
| 2 | 3.13msec | 100msec | XC61xxA3xxxx | H | 100msec | 100msec | XC61xxD3xxxx |
| 3 | 3.13msec | 200msec | XC61xxA4xxxx | K | 100msec | 200msec | XC61xxD4xxxx |
| 4 | 3.13msec | 400msec | XC61xxA5xxxx | L | 100msec | 400msec | XC61xxD5xxxx |
| 5 | 3.13msec | 1.6sec | XC61xxA6xxxx | M | 100msec | 1.6sec | XC61xxD6xxxx |
| B | 25msec | XC61X6, XC61X7 series | XC61xxB0xxxx | E | 200msec | XC61X6, XC61X7 series | XC61xxE0xxxx |
| 6 | 25msec | 50msec | XC61xxB2xxxx | P | 200msec | 200msec | XC61xxE4xxxx |
| 7 | 25msec | 100msec | XC61xxB3xxxx | R | 200msec | 400msec | XC61xxE5xxxx |
| 8 | 25msec | 200msec | XC61xxB4xxxx | S | 200msec | 1.6sec | XC61xxE6xxxx |
| 9 | 25msec | 400msec | XC61xxB5xxxx | F | 400msec | XC61X6, XC61X7 series | XC61xxF0xxxx |
| A | 25msec | 1.6sec | XC61xxB6xxxx | T | 400msec | 400msec | XC61xxF5xxxx |
| C | 50msec | XC61X6, XC61X7 series | XC61xxC0xxxx | U | 400msec | 1.6sec | XC61xxF6xxxx |
| B | 50msec | 50msec | XC61xxC2xxxx | H | 1.6sec | XC61X6, XC61X7 series | XC61xxH0xxxx |
| C | 50msec | 100msec | XC61xxC3xxxx | V | 1.6sec | 1.6sec | XC61xxH6xxxx |
| D | 50msec | 200msec | XC61xxC4xxxx | | | | |

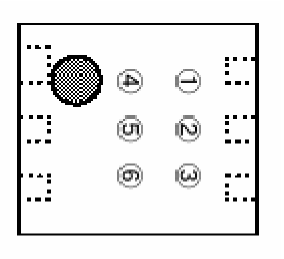
③ Represents detect voltage

| MARK | DETECT VOLTAGE | PRODUCT SERIES | MARK | DETECT VOLTAGE | PRODUCT SERIES |
|---|---|---|---|---|---|
| F | 1.6 | XC61Xxxx16xx | 3 | 3.4 | XC61Xxxx34xx |
| H | 1.7 | XC61Xxxx17xx | 4 | 3.5 | XC61Xxxx35xx |
| K | 1.8 | XC61Xxxx18xx | 5 | 3.6 | XC61Xxxx36xx |
| L | 1.9 | XC61Xxxx19xx | 6 | 3.7 | XC61Xxxx37xx |
| M | 2.0 | XC61Xxxx20xx | 7 | 3.8 | XC61Xxxx38xx |
| N | 2.1 | XC61Xxxx21xx | 8 | 3.9 | XC61Xxxx39xx |
| P | 2.2 | XC61Xxxx22xx | 9 | 4.0 | XC61Xxxx40xx |
| R | 2.3 | XC61Xxxx23xx | A | 4.1 | XC61Xxxx41xx |
| S | 2.4 | XC61Xxxx24xx | B | 4.2 | XC61Xxxx42xx |
| T | 2.5 | XC61Xxxx25xx | C | 4.3 | XC61Xxxx43xx |
| U | 2.6 | XC61Xxxx26xx | D | 4.4 | XC61Xxxx44xx |
| V | 2.7 | XC61Xxxx27xx | E | 4.5 | XC61Xxxx45xx |
| X | 2.8 | XC61Xxxx28xx | F | 4.6 | XC61Xxxx46xx |
| Y | 2.9 | XC61Xxxx29xx | H | 4.7 | XC61Xxxx47xx |
| Z | 3.0 | XC61Xxxx30xx | K | 4.8 | XC61Xxxx48xx |
| 0 | 3.1 | XC61Xxxx31xx | L | 4.9 | XC61Xxxx49xx |
| 1 | 3.2 | XC61Xxxx32xx | M | 5.0 | XC61Xxxx50xx |
| 2 | 3.3 | XC61Xxxx33xx | | | |

④ Represents production lot number
0 to 9 and A to Z and inverted 0 to 9 and A to Z repeated. (G, I, J, O, Q, W expected.)
* 'X' represents both '0' and '1'. (ex. XC61X1⇒XC6101 and XC6111)

## ■MARKING RULE (Continued)

●USP-6C




USP-6C
(TOP VIEW)

① Represents product series

| MARK | PRODUCT SERIES | MARK | PRODUCT SERIES |
|---|---|---|---|
| 3 | XC6101xxxxxx | 8 | XC6111xxxxxx |
| 4 | XC6102xxxxxx | 9 | XC6112xxxxxx |
| 5 | XC6103xxxxxx | A | XC6113xxxxxx |
| 6 | XC6104xxxxxx | B | XC6114xxxxxx |
| 7 | XC6105xxxxxx | C | XC6115xxxxxx |
| 3 | XC6106xxxxxx | 8 | XC6116xxxxxx |
| 4 | XC6107xxxxxx | 9 | XC6117xxxxxx |

② Represents release delay time

| MARK | RELEASE DELAY TIME | PRODUCT SERIES |
|---|---|---|
| A | 3.13msec | XC61XxAxxxxx |
| B | 25msec | XC61XxBxxxxx |
| C | 50msec | XC61XxCxxxxx |
| D | 100msec | XC61XxDxxxxx |
| E | 200msec | XC61XxExxxxx |
| F | 400msec | XC61XxFxxxxx |
| H | 1.6sec | XC61XxHxxxxx |

③ Represents watchdog timeout period

| MARK | WATCHDOG TIMEOUT PERIOD | PRODUCT SERIES |
|---|---|---|
| 0 | XC61X6, XC61X7 series | XC61Xxx0xxxx |
| 1 | 6.25msec | XC61Xxx1xxxx |
| 2 | 50msec | XC61Xxx2xxxx |
| 3 | 100msec | XC61Xxx3xxxx |
| 4 | 200msec | XC61Xxx4xxxx |
| 5 | 400msec | XC61Xxx5xxxx |
| 6 | 1.6sec | XC61Xxx6xxxx |

④⑤ Represents detect voltage

| MARK | | DETECT VOLTAGE (V) | PRODUCT SERIES |
|---|---|---|---|
| ④ | ⑤ | | |
| 3 | 3 | 3.3 | XC61Xxxx33xx |
| 5 | 0 | 5.0 | XC61Xxxx50xx |

⑥ Represents production lot number

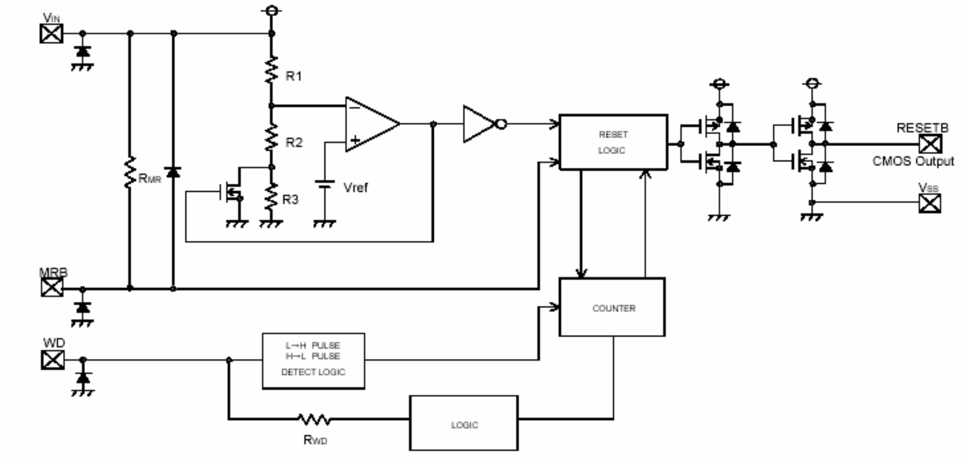
0 to 9 and A to Z repeated.　(G, I, J, O, Q, W excepted.)

* No character inversion used.

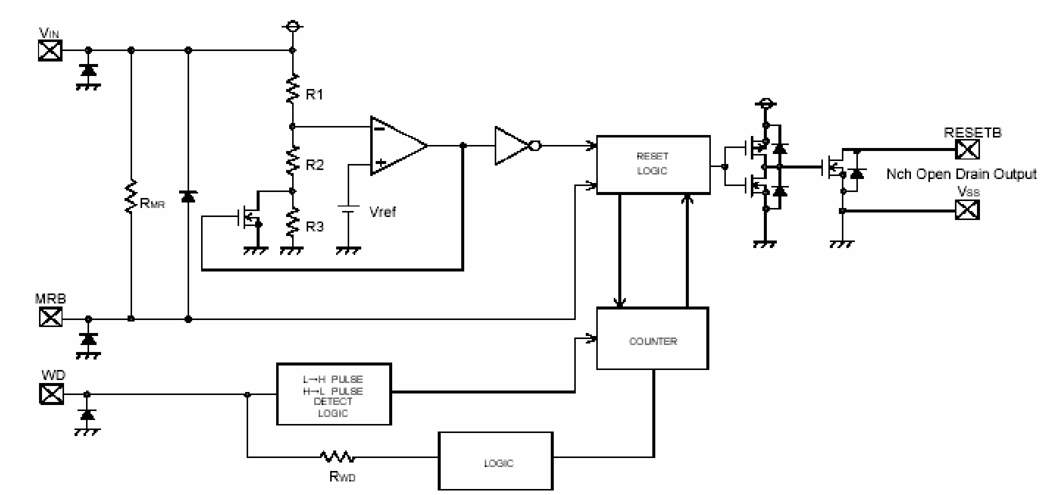
** ‘X’ represents both ‘0’ and ‘1’. (ex. XC61X1⇒XC6101 and XC6111)

# ■BLOCK DIAGRAMS

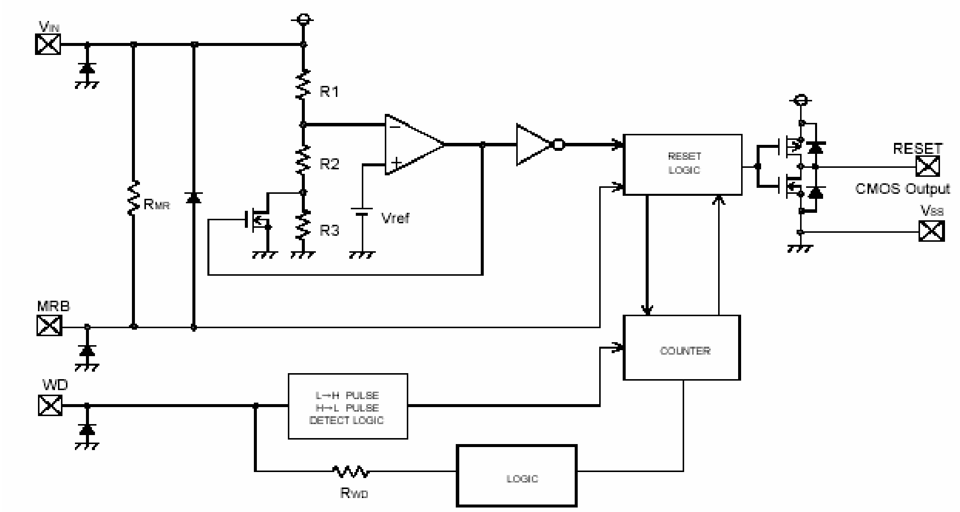
●XC6101, XC6111 Series




●XC6102, XC6112 Series

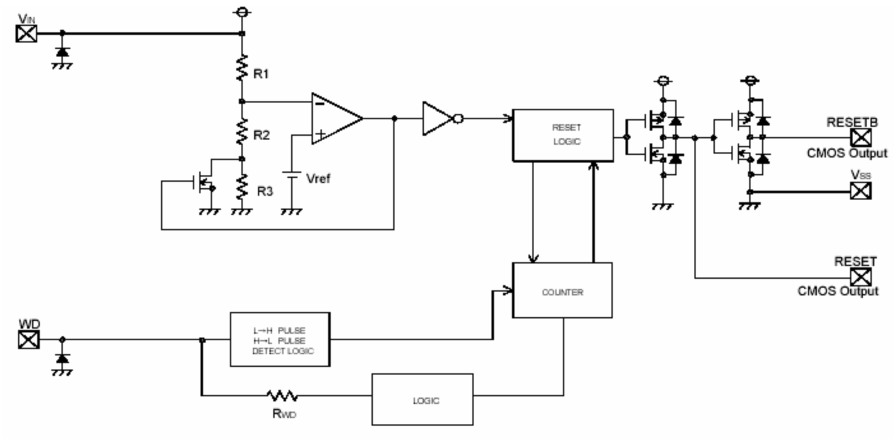



●XC6103, XC6113 Series

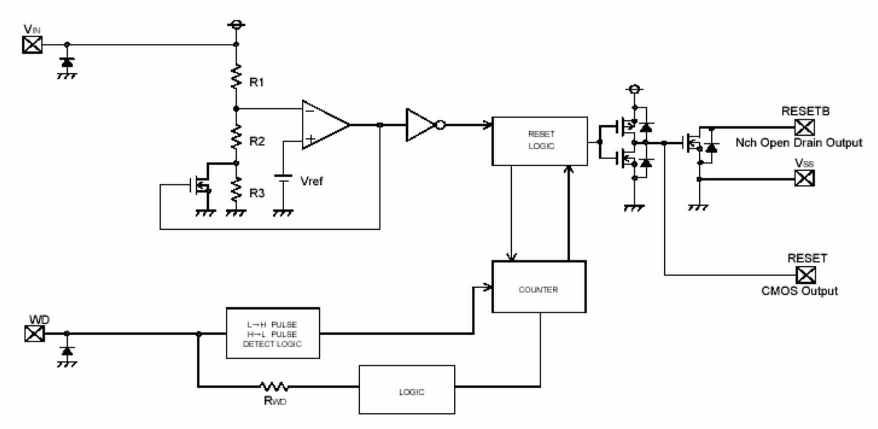


## ■BLOCK DIAGRAMS (Continued)

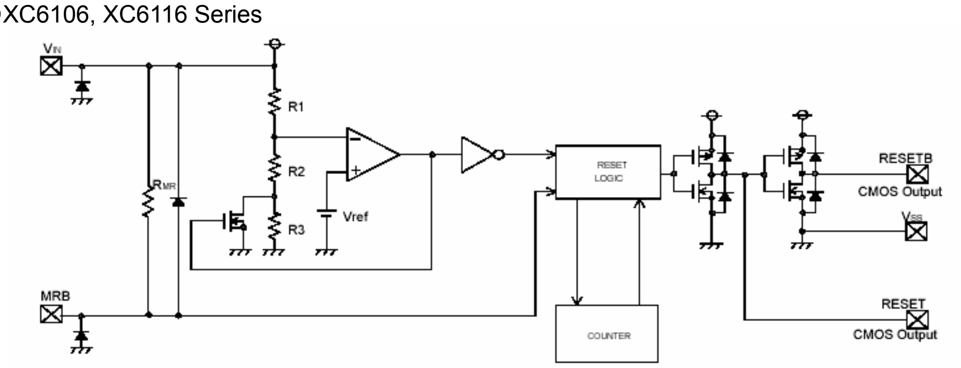
●XC6104, XC6114 Series



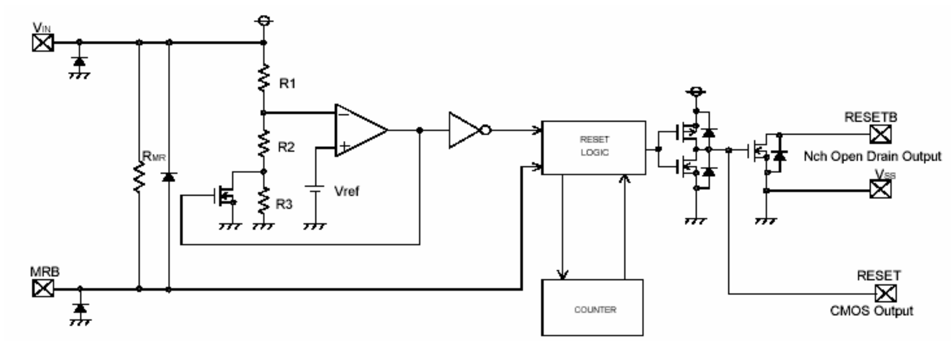

●XC6105, XC6115 Series




●XC6106, XC6116 Series




●XC6107, XC6117 Series



## ■ABSOLUTE MAXIMUM RATINGS

Ta = 25°C

| PARAMETER | | SYMBOL | RATINGS | UNITS |
|---|---|---|---|---|
| Input Voltage | | $V_{IN}$ | $V_{SS}$ -0.3 ~ 7.0 | V |
| | | $M_{RB}$ | $V_{SS}$ -0.3 ~ $V_{IN}$ +0.3 | V |
| | | WD | $V_{SS}$ -0.3 ~ 7.0 | V |
| Output Current | | $I_{OUT}$ | 20 | mA |
| Output Voltage | CMOS Output | RESETB/RESET | $V_{SS}$ -0.3 ~ $V_{IN}$ +0.3 | V |
| | N-ch Open Drain Output | RESETB | $V_{SS}$ -0.3 ~ 7.0 | |
| Power Dissipation | SOT-25 | Pd | 250 | mW |
| | USP-6C | | 100 | |
| Operational Temperature Range | | Topr | -40 ~ +85 | °C |
| Storage Temperature Range | | Tstg | -40 ~ +125 | °C |

# ■ELECTRICAL CHARACTERISTICS

●XC6101~XC6107, XC6111~XC6117 Series

Ta = 25 °C

| PARAMETER | SYMBOL | CONDITIONS | | MIN. | TYP. | MAX. | UNITS | CIRCUIT |
|---|---|---|---|---|---|---|---|---|
| Detect Voltage | $V_{DFL}$ $V_{DFH}$ | | | $V_{DF(T)}$ × 0.98 | $V_{DF(T)}$ | $V_{DF(T)}$ × 1.02 | V | 1 |
| Hysteresis Range XC6101~XC6107 (*1) | $V_{HYS}$ | | | $V_{DF}$ × 0.02 | $V_{DF}$ × 0.05 | $V_{DF}$ × 0.08 | V | 1 |
| Hysteresis Range XC6111~XC6117 (*2) | $V_{HYS}$ | | | 0 | $V_{DF}$ × 0.001 | $V_{DF}$ x 0.01 | V | 1 |
| Supply Current | $I_{SS}$ | XC61X1/XC61X2/XC61X3 XC61X4/XC61X5 (*3) (The MRB & the WD Pin: No connection) | $V_{IN}=V_{DF(T)}×0.9V$ | - | 5 | 11 | μA | 2 |
| | | | $V_{IN}=V_{DF(T)}×1.1V$ | - | 10 | 16 | | |
| | | | $V_{IN}$=6.0V | - | 12 | 18 | | |
| | | XC61X6/XC61X7 (*3) (The MRB Pin: No connection) | $V_{IN}=V_{DF(T)}×0.9V$ | - | 4 | 10 | | |
| | | | $V_{IN}=V_{DF(T)}×1.1V$ | - | 8 | 14 | | |
| | | | $V_{IN}$=6.0V | - | 10 | 16 | | |
| Operating Voltage | $V_{IN}$ | | | 1.0 | - | 6.0 | V | 1 |
| $V_{DFL}$ Output Current (RESETB) | $I_{RBOUT}$ | N-ch. $V_{DS}$ = 0.5V | VIN=1.0V | 0.15 | 0.5 | - | mA | 3 |
| | | | $V_{IN}$=2.0V ($V_{DFL(T)}$> 2.0V) | 2.0 | 2.5 | - | | |
| | | | $V_{IN}$=3.0V ($V_{DFL(T)}$ >3.0V) | 3.0 | 3.5 | - | | |
| | | | $V_{IN}$=4.0V ($V_{DFL(T)}$ >4.0V) | 3.5 | 4.0 | - | | |
| | | CMOS, P-ch $V_{DS}$ = 0.5V | $V_{IN}$=6.0V | - | - 1.1 | -0.8 | | 4 |
| $V_{DFH}$ Output Current (RESET) | $I_{ROUT}$ | N-ch $V_{DS}$ = 0.5V | $V_{IN}$=6.0V | 4.4 | 4.9 | - | mA | 3 |
| | | P-ch. $V_{DS}$ = 0.5V | $V_{IN}$=1.0V | - | - 0.08 | - 0.02 | | 4 |
| | | | $V_{IN}$=2.0V ($V_{DFH(T)}$> 2.0V) | - | - 0.50 | - 0.30 | | |
| | | | $V_{IN}$=3.0V ($V_{DFH(T)}$>3.0V) | - | - 0.75 | - 0.55 | | |
| | | | $V_{IN}$=4.0V ($V_{DFH(T)}$>4.0V) | - | - 0.95 | - 0.75 | | |
| Temperature Characteristics | $\Delta V_{DF}$ / $\Delta Topr \cdot V_{DF}$ | -40°C ≦ Topr ≦ 85 °C | | - | ±100 | - | ppm / °C | 1 |
| Release Delay Time ($V_{DF}$≦1.8V) | $T_{DR}$ | Time until $V_{IN}$ is increased from 1.0V to 2.0V and attains to the release time level, and the Reset output pin inverts. | | 2 | 3.13 | 5 | ms | 5 |
| | | | | 13 | 25 | 38 | | |
| | | | | 25 | 50 | 75 | | |
| | | | | 60 | 100 | 140 | | |
| | | | | 120 | 200 | 280 | | |
| | | | | 240 | 400 | 560 | | |
| | | | | 960 | 1600 | 2240 | | |
| Release Delay Time ($V_{DF}$≧1.9V) | $T_{DR}$ | Time until $V_{IN}$ is increased from 1.0V to ($V_{DF}$x1.1V) and attains to the release time level, and the Reset output pin inverts. | | 2 | 3.13 | 5 | ms | 5 |
| | | | | 13 | 25 | 38 | | |
| | | | | 25 | 50 | 75 | | |
| | | | | 60 | 100 | 140 | | |
| | | | | 120 | 200 | 280 | | |
| | | | | 240 | 400 | 560 | | |
| | | | | 960 | 1600 | 2240 | | |
| Detect Delay Time | $T_{DF}$ | Time until $V_{IN}$ is decreased from 6.0V to 1.0V and attains to the detect voltage level, and the Reset output pin detects while the WD pin left opened. | | - | 3 | 30 | μs | 5 |
| $V_{DFL}$/$V_{DFH}$ CMOS Output Leak Current | $I_{LEAK}$ | $V_{IN}$=6.0V, RESETB=6.0V ($V_{DFL}$) $V_{IN}$=6.0V, RESET=0V ($V_{DFH}$) | | - | 0.01 | - | μA | 3 |
| $V_{DFL}$ N-ch Open Drain Output Leak Current | $I_{LEAK}$ | $V_{IN}$=6.0V, RESETB=6.0V | | - | 0.01 | 0.10 | μA | 3 |

NOTE:
*1: XC6101~XC6107 (with hysteresis)
*2: XC6111~XC6117 (without hysteresis)
*3: ‘X’ represents both ‘0’ and ‘1’. (ex. XC61X1⇒XC6101 and XC6111)
*4: $V_{DF(T)}$: Setting detect voltage
*5: If only “$V_{DF}$” is indicated, it represents both $V_{DFL}$ (low when detected) and $V_{DFH}$ (high when detected).

# ■ELECTRICAL CHARACTERISTICS (Continued)

●XC6101~XC6105, XC6111~XC6115 Series

Ta = 25 °C

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS | CIRCUIT |
|---|---|---|---|---|---|---|---|
| Watchdog Timeout Period ($V_{DF}$≦1.8V) | $T_{WD}$ | Time until $V_{IN}$ increases form 1.0V to 2.0V and the Reset output pin is released to go into the detection state. (WD=$V_{SS}$) | 3.13 | 6.25 | 9.38 | ms | 6 |
| | | | 25 | 50 | 75 | | |
| | | | 60 | 100 | 140 | | |
| | | | 120 | 200 | 280 | | |
| | | | 240 | 400 | 560 | | |
| | | | 960 | 1600 | 2240 | | |
| Watchdog Timeout Period ($V_{DF}$≧1.9V) | $T_{WD}$ | Time until $V_{IN}$ increases form 1.0V to ($V_{DF}$x1.1V) and the Reset output pin is released to go into the detection state. (WD=$V_{SS}$) | 3.13 | 6.25 | 9.38 | ms | 6 |
| | | | 25 | 50 | 75 | | |
| | | | 60 | 100 | 140 | | |
| | | | 120 | 200 | 280 | | |
| | | | 240 | 400 | 560 | | |
| | | | 960 | 1600 | 2240 | | |
| Watchdog Minimum Pulse Width | $T_{WDIN}$ | $V_{IN}$=6.0V, Apply pulse from 6.0V to 0V to the WD pin. | 300 | - | - | ns | 7 |
| Watchdog High Level Voltage | $V_{WDH}$ | $V_{IN}$=$V_{DF}$ x 1.1V ~ 6.0V | $V_{IN}$ x 0.7 | - | 6 | V | 7 |
| Watchdog Low Level Voltage | $V_{WDL}$ | $V_{IN}$=$V_{DF}$ x 1.1V ~ 6.0V | 0 | - | $V_{IN}$ x 0.3 | V | 7 |
| Watchdog Input Current | $I_{WD}$ | $V_{IN}$=6.0V, $V_{WD}$=6.0V (Avg. when peak ) | - | 12 | 19 | μA | 8 |
| | | $V_{IN}$=6.0V, $V_{WD}$=0V (Avg. when peak) | - 19 | -12 | - | | |
| Watchdog Input Resistance | $R_{WD}$ | $V_{IN}$=6.0V, $V_{WD}$=0V, $R_{WD}$=$V_{IN}$/ \|$I_{WD}$\| | 315 | 500 | 880 | kΩ | 8 |

●XC6101 ~ XC6103, XC6106 ~ XC6107, XC6111 ~ XC6113, XC6116 ~ XC6117 Series

Ta = 25 °C

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS | CIRCUIT |
|---|---|---|---|---|---|---|---|
| MRB High Level Voltage | $V_{MRH}$ | $V_{IN}$=$V_{DF}$x1.1V ~ 6.0V | 1.4 | - | $V_{IN}$ | V | 9 |
| MRB Low Level Voltage | $V_{MRL}$ | $V_{IN}$=$V_{DF}$x1.1V ~ 6.0V | 0 | - | 0.35 | | 9 |
| MRB Pull-up Resistance | $R_{MR}$ | $V_{IN}$=6.0V, MRB=0V, $R_{MR}$=$V_{IN}$/ \|$I_{MRB}$\| | 1.6 | 2.4 | 3.0 | MΩ | 10 |
| MRB Minimum Pulse Width (*3) XC6101~XC6105 XC6111~XC6115 | $T_{MRIN}$ | $V_{IN}$=6.0V, Apply pulse from 6.0V to 0V to the MRB pin | 2.8 | - | - | μs | 11 |
| MRB Minimum Pulse Width (*4) XC6106, XC6107 XC6116, XC6117 | $T_{MRIN}$ | $V_{IN}$=6.0V, Apply pulse from 6.0V to 0V to the MRB pin | 1.2 | - | - | | |

NOTE:
*1: $V_{DF(T)}$: Setting detect voltage
*2: If only "$V_{DF}$" is indicated, it represents both $V_{DFL}$ (low when detected) and $V_{DFH}$ (high when detected).
*3: Watchdog function is available.
*4: Watchdog function is not available.

## ■OPERATIONAL EXPLANATION

The XC6101~XC6107, XC6111~XC6117 series compare, using the error amplifier, the voltage of the internal voltage reference source with the voltage divided by R1, R2 and R3 connected to the $V_{IN}$ pin. The resulting output signal from the error amplifier activates the watchdog logic, manual reset logic, delay circuit and the output driver. When the $V_{IN}$ pin voltage gradually falls and finally reaches the detect voltage, the RESETB pin output goes from high to low in the case of the $V_{DFL}$ type ICs, and the RESET pin output goes from low to high in the case of the $V_{DFH}$ type ICs.

<RESETB / RESET Pin Output Signal>
* $V_{DFL}$ (RESETB) type - output signal: Low when detected.
The RESETB pin output goes from high to low whenever the $V_{IN}$ pin voltage falls below the detect voltage, or whenever the MRB pin is driven from high to low. The RESETB pin remains low for the release delay time ($T_{DR}$) after the $V_{IN}$ pin voltage reaches the release voltage. If neither rising nor falling signals are applied to the WD pin within the watchdog timeout period, the RESETB pin output remains low for the release delay time ($T_{DR}$), and thereafter the RESET pin outputs high level signal.

* $V_{DFH}$ (RESET) type – output signal: High when detected.
The RESET pin output goes from low to high whenever the $V_{IN}$ pin voltage falls below the detect voltage, or whenever the MRB pin is driven from high to low. The RESET pin remains high for the release delay time ($T_{DR}$) after the $V_{IN}$ pin voltage reaches the release voltage. If neither rising nor falling signals are applied to the WD pin within the watchdog timeout period, the $V_{OUT}$ pin output remains high for the release delay time ($T_{DR}$), and thereafter the RESET pin outputs low level signal.

<Hysteresis>
When the internal comparator output is high, the NMOS transistor connected in parallel to R3 is turned ON, activating the hysteresis circuit. The difference between the release and detect voltages represents the hysteresis range, as shown by the following calculations:

*$V_{DF}$ (detect voltage) = (R1+R2+R3) x Vref(R2+R3)*
*$V_{DR}$ (release voltage) = (R1+R2) x Vref(R2)*
*$V_{HYS}$ (hysteresis range)=$V_{DR}$-$V_{DF}$ (V)*
*$V_{DR} > V_{DF}$*
* *Detect voltage ($V_{DF}$) includes conditions of both $V_{DFL}$ (low when detected) and $V_{DFH}$ (high when detected).*
* *Please refer to the block diagrams for R1, R2, R3 and Vref.*

Hysteresis range is selectable from $V_{DF}$ x 0.05V (XC6101~XC6107) or $V_{DF}$ x 0.001V (XC6111~XC6117).

<Watchdog (WD) Pin>
The XC6101~XC6107, XC6111~XC6117 series use a watchdog timer to detect malfunction or “runaway” of the microprocessor. If neither rising nor falling signals are applied from the microprocessor within the watchdog timeout period, the RESETB/RESET pin output maintains the detection state for the release delay time ($T_{DR}$), and thereafter the RESET/RESETB pin output returns to the release state (Please refer to the FUNCTION CHART). The timer in the watchdog is then restarted. Six watchdog timeout period settings are available in 1.6sec, 400msec, 200msec, 100msec, 50msec, 6.25msec.

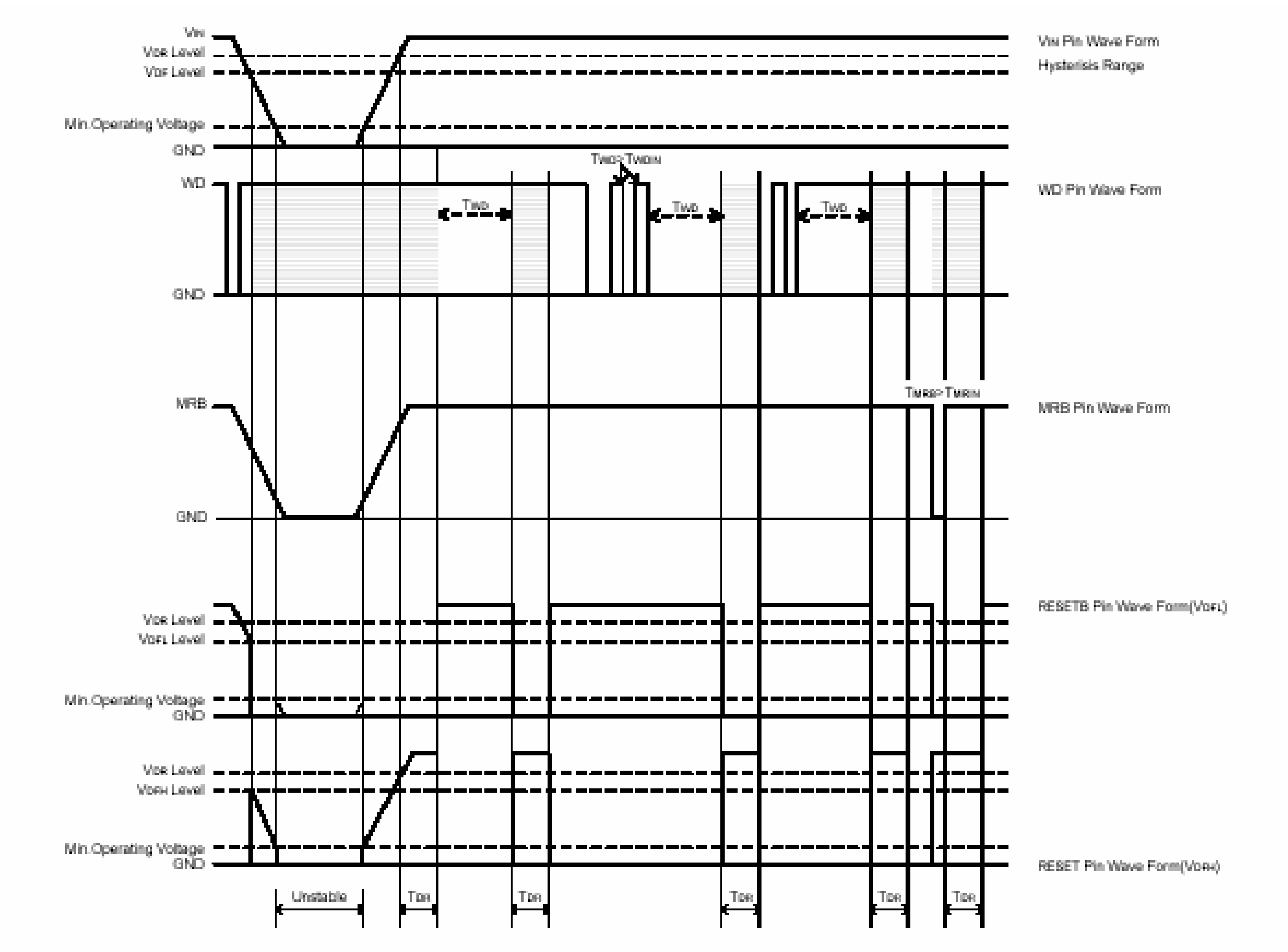
<MRB Pin>
Using the MRB pin input, the RESET/RESETB pin signal can be forced to the detection state. When the MRB pin is driven from high to low, the RESETB pin output goes from high to low in the case of the $V_{DFL}$ type ICs, and the RESET pin output goes from low to high in the case of the $V_{DFH}$ type. Even after the MRB pin is driven back high, the RESET/RESETB pin output maintains the detection state for the release delay time ($T_{DR}$). Since the MRB pin is internally pulled up to the $V_{IN}$ pin voltage level, leave the MRB pin open if unused (Please refer to the FUNCTION CHART). A diode, which is an input protection element, is connected between the MRB pin and $V_{IN}$ pin. Therefore, if the MRB pin is applied voltage that exceeds $V_{IN}$, the current will flow to $V_{IN}$ through the diode. Please use this IC within the stated maximum ratings ($V_{SS}$ -0.3 ~ $V_{IN}$ +0.3) on the MRB pin.

<Release Delay Time>
Release delay time ($T_{DR}$) is the time that elapses from when the $V_{IN}$ pin reaches the release voltage, or when the watchdog timeout period expires with no rising signal applied to the WD pin, until the RESET/RESETB pin output is released from the detection state. Seven release delay time ($T_{DR}$) watchdog timeout period settings are available in 1.6sec, 400msec, 200msec, 100msec, 50msec, 25msec, 3.13msec.

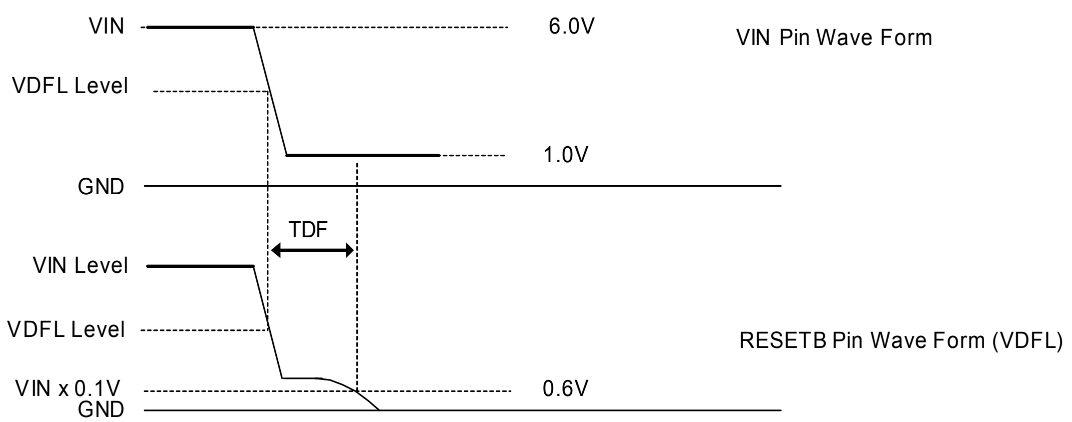
<Detect Delay Time>
Detect Delay Time ($T_{DF}$) is the time that elapses from when the $V_{IN}$ pin voltage falls to the detect voltage until the RESET/ RESETB pin output goes into the detection state.

# ■TIMING CHARTS

●CMOS Output




●TDF (CMOS Output)



## ■NOTES ON USE

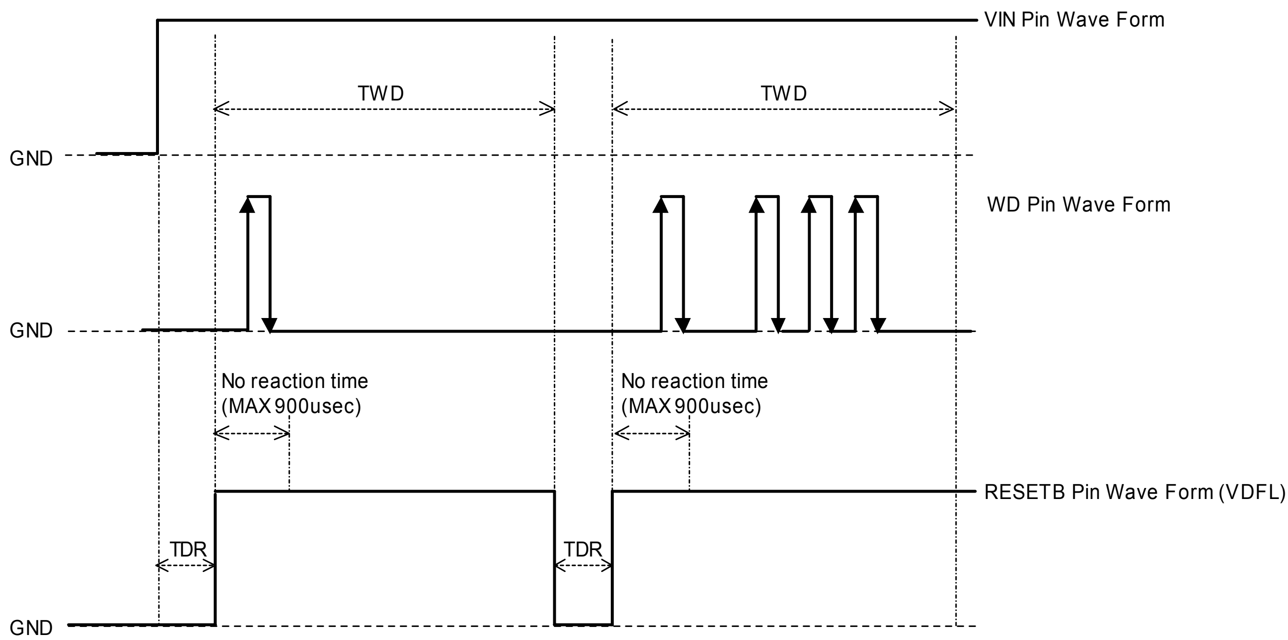
1. Please use this IC within the stated maximum ratings. Operation beyond these limits may cause degrading or permanent damage to the device.

2. When a resistor is connected between the $V_{IN}$ pin and the input, the $V_{IN}$ voltage drops while the IC is operating and a malfunction may occur as a result of the IC's through current. For the CMOS output products, the $V_{IN}$ voltage drops while the IC is operating and malfunction may occur as a result of the IC's output current. Please be careful with using the XC6111~XC6117 series (without hysteresis).

3. In order to stabilize the IC's operations, please ensure that the $V_{IN}$ pin's input frequency's rise and fall times are more than 1 μ sec/V.

4. Noise at the power supply may cause a malfunction of the watchdog operation or the circuit. In such case, please strength the line between $V_{IN}$ and the GND pin and connect about 0.22μF of a capacitor between the $V_{IN}$ pin and the GND pin.

5. Protecting against a malfunction while the watchdog time out period, an ignoring time (no reaction time) occurs to the rise and fall times. Referring to the figure below, the ignoring time (no reaction time) lasts for 900μsec at maximum.



## ■PIN LOGIC CONDITIONS

| PIN NAME | LOGIC | CONDITIONS |
|---|---|---|
| $V_{IN}$ | H | $V_{IN} \geqq V_{DF}+V_{HYS}$ |
| | L | $V_{IN} \leqq V_{DF}$ |
| MRB | H | MRB$\geqq$1.40V |
| | L | MRB$\leqq$0.35V |
| WD | H | When keeping $W_D \geqq V_{WDH}$ more than $T_{WD}$ |
| | L | When keeping $W_D \leqq V_{WDL}$ more than $T_{WD}$ |
| | L → H | $V_{WDL} \rightarrow V_{WDH}$, $T_{WDIN} \geqq$300nsec |
| | H → L | $V_{WDH} \rightarrow V_{WDH}$, $T_{WDIN} \geqq$300nsec |

NOTE:
*1: If only "$V_{DF}$" is indicated, it represents both $V_{DFL}$ (low when detected) and $V_{DFH}$ (high when detected).
*2: For the details of each parameter, please see the electrical characteristics.
$V_{DF}$: Detect Voltage
$V_{HYS}$: Hysteresis Range
$V_{WDH}$: WD High Level Voltage
$V_{WDL}$: WD Low Level Voltage
$T_{WDIN}$: WD Pulse Width
$T_{WD}$: WD Timeout Period

## ■FUNCTION CHART

●XC6101/XC61111, XC6102/6112 Series

| $V_{IN}$ | MRB | WD | RESETB (*2) |
|---|---|---|---|
| H | H or Open | H | Repeat detect and release (H→L→H) |
| H | | L | |
| H | | Open | H |
| H | | L → H | |
| H | | H → L | |
| H | L | *1 | L |
| L | | | |

●XC6103/XC61113 Series

| $V_{IN}$ | MRB | WD | RESETB (*3) |
|---|---|---|---|
| H | H or Open | H | Repeat detect and release (L→H→L) |
| H | | L | |
| H | | Open | L |
| H | | L → H | |
| H | | H → L | |
| H | L | *1 | H |
| L | | | |

●XC6104/XC61114, XC6105/XC6115 Series

| $V_{IN}$ | WD | RESETB (*2) | RESET (*3) |
|---|---|---|---|
| H | H | Repeat detect and release (H→L→H) | Repeat detect and release (L→H→L) |
| H | L | | |
| H | Open | H | L |
| H | L → H | | |
| H | H → L | | |
| H | *1 | L | H |
| L | | | |

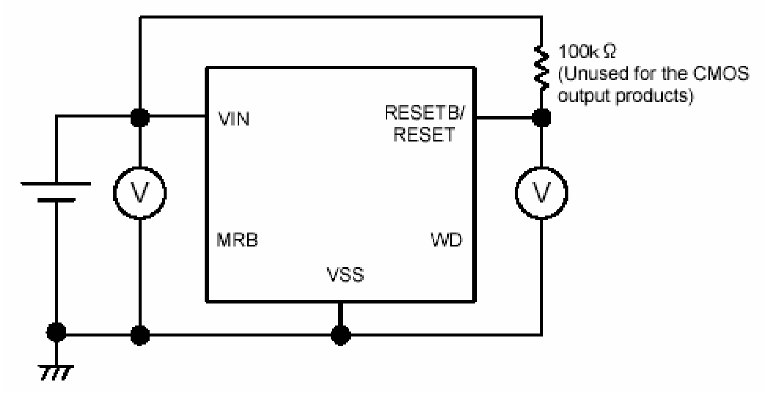
●XC6106/XC61116, XC6107/XC6117 Series

| $V_{IN}$ | MRB | RESETB (*2) | RESET (*3) |
|---|---|---|---|
| H | H or Open | H | L |
| H | L | L | H |
| L | | | |

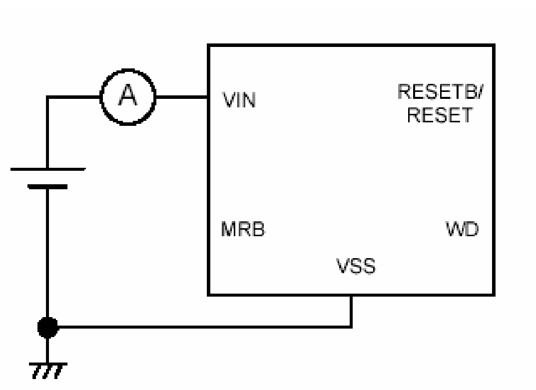
*1: Including all logic of WD (WD=H, L, L→H, H→L, OPEN).
*2: When the RESETB is High, the circuit is in the release state.
When the RESETB is Low, the circuit is in the detection state.
*3: When the RESET is High, the circuit is in the release state.
When the RESET is Low, the circuit is in the detection state.
*4: $V_{IN}$=L and MRB=H can not be combined for the rated input voltage of the MRB pin is Vss-0.3V to $V_{IN}$+0.3V.
*5: The RESET/RESETB pin becomes indefinite operation while 0.35V<MRB<1.4V.

## ■TEST CIRCUITS

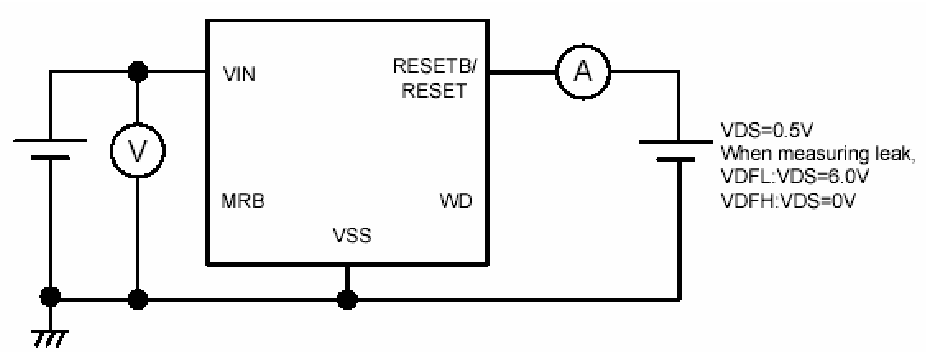
Circuit 1



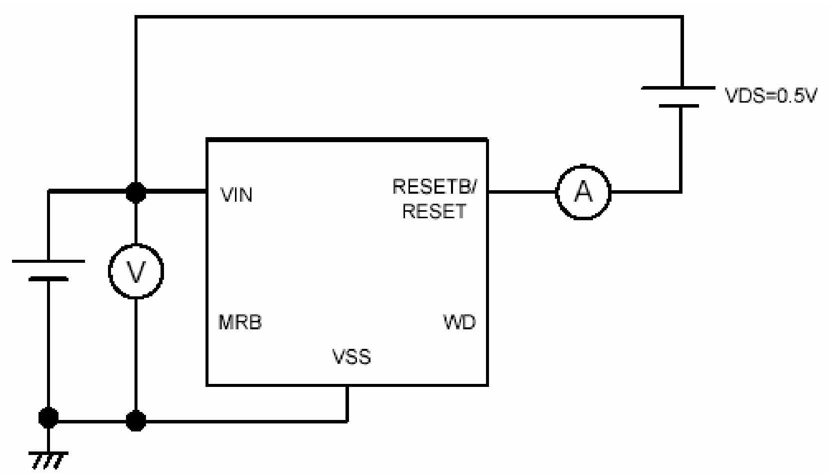

Circuit 2




Circuit 3

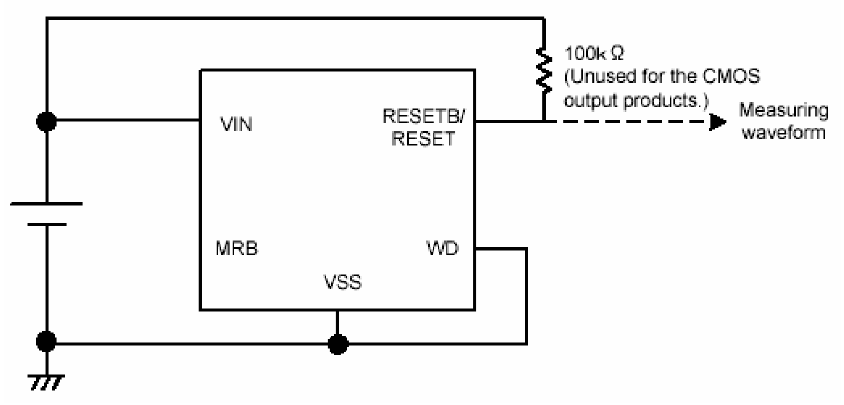



Circuit 4

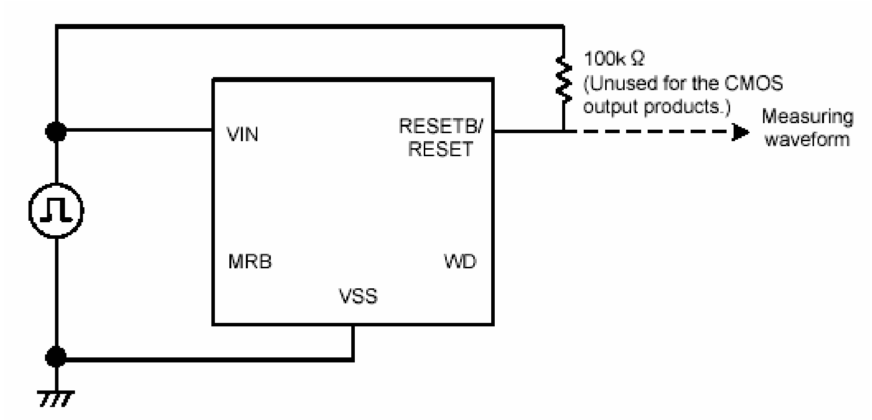


## ■TEST CIRCUITS (Continued)

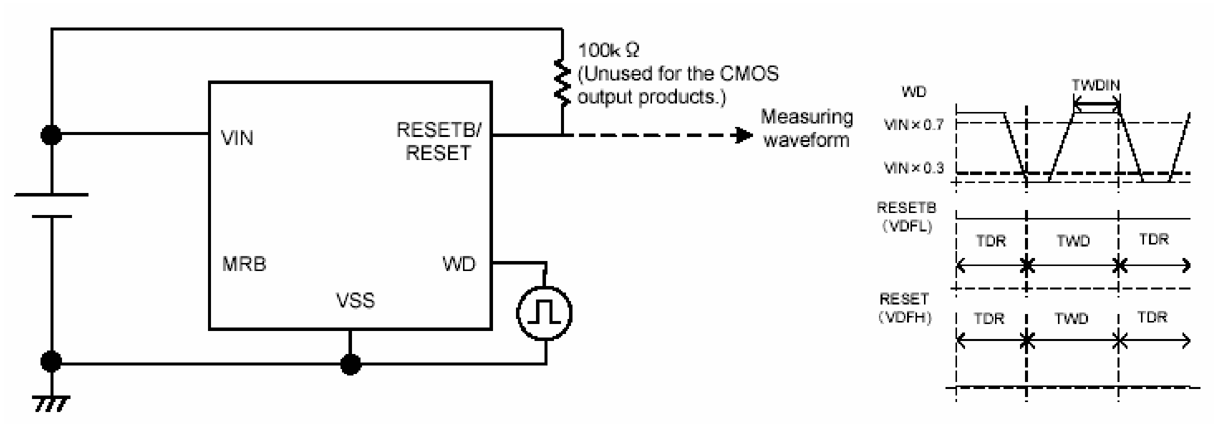
Circuit 5




Circuit 6

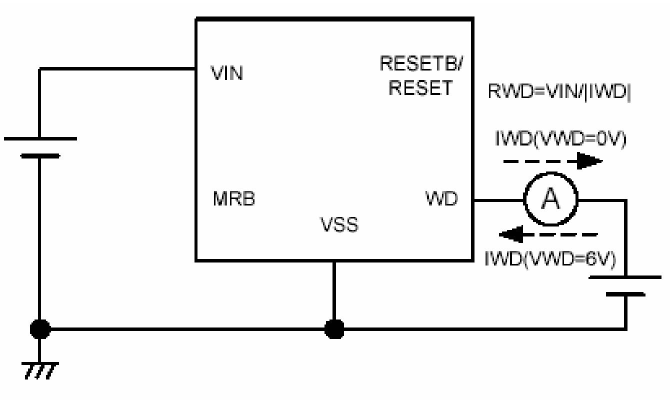



Circuit 7

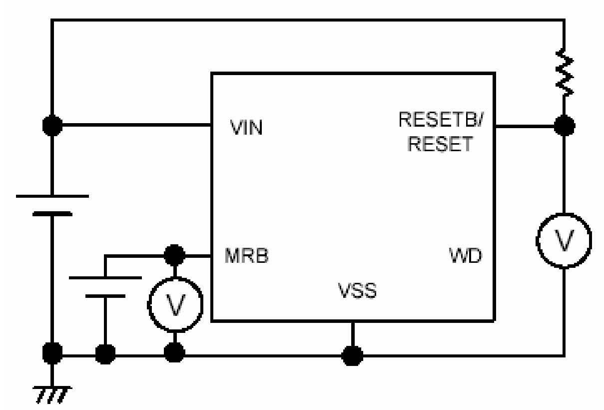


## ■TEST CIRCUITS (Continued)

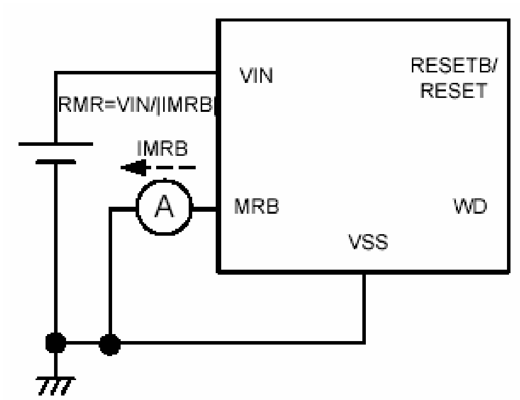
Circuit 8



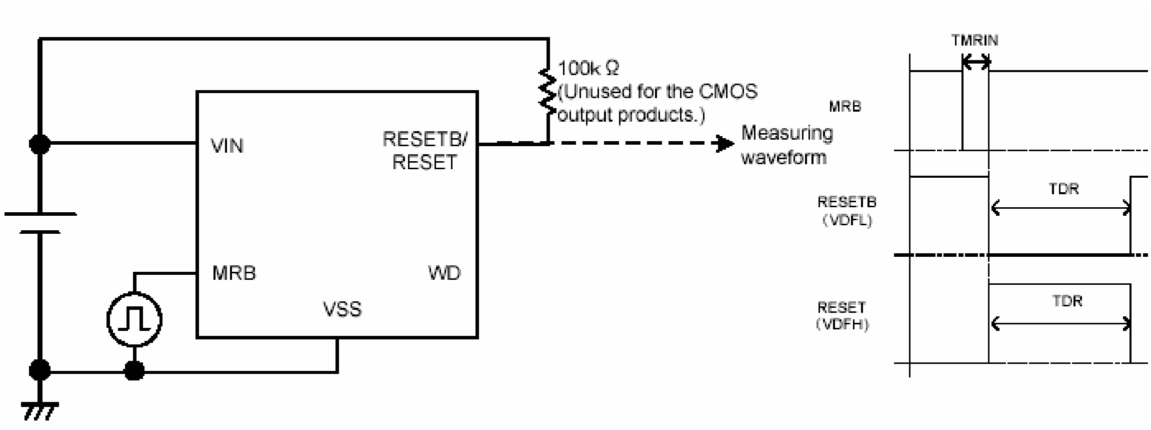

Circuit 9




Circuit 10

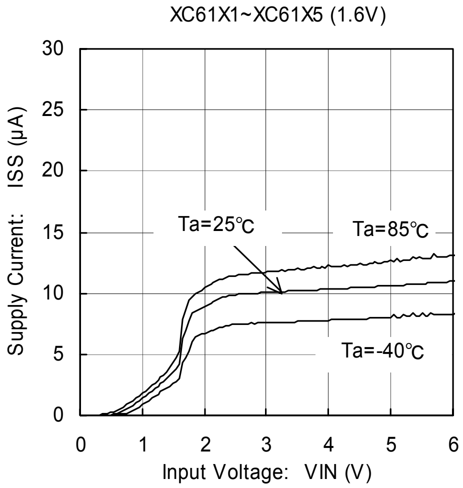


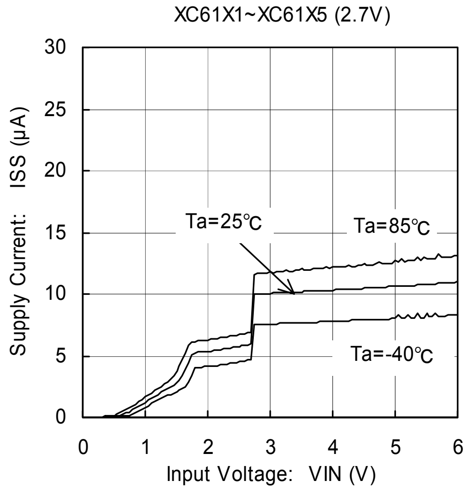

Circuit 11

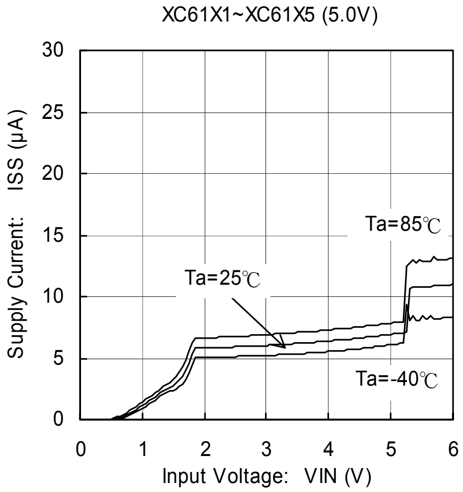


# ■TYPICAL PERFORMANCE CHARACTERISTICS

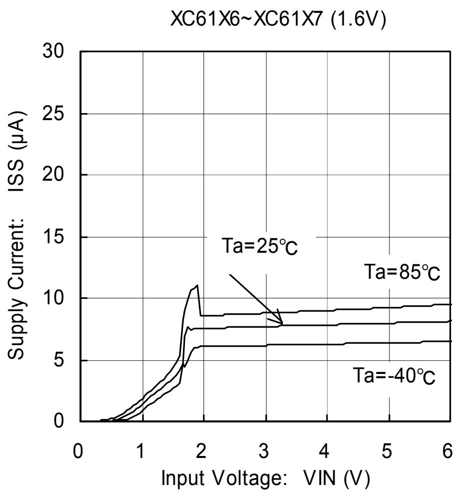
(1.1) Supply Current vs. Input Voltage

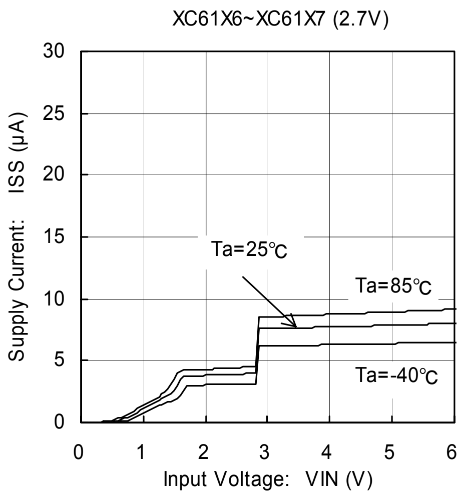



(1.2) Supply Current vs. Input Voltage

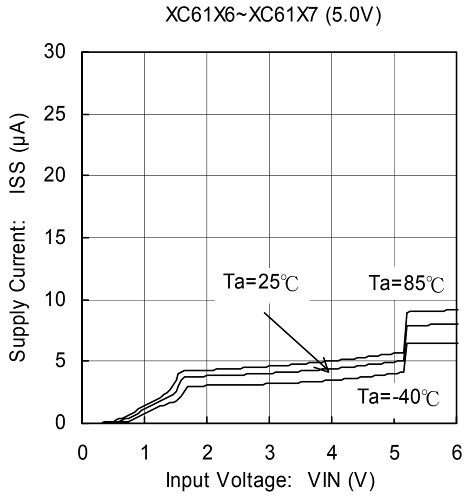


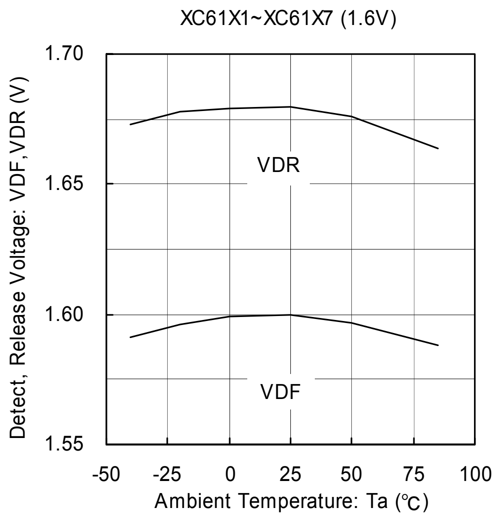

* ‘X’ represents both ‘0’ and ‘1’. (ex. XC61X1⇒XC6101 and XC6111)

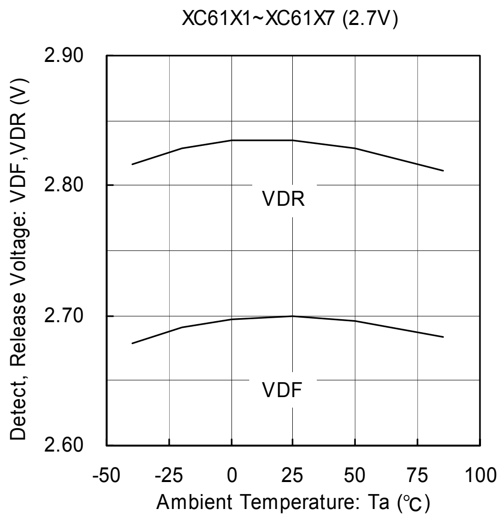
## ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

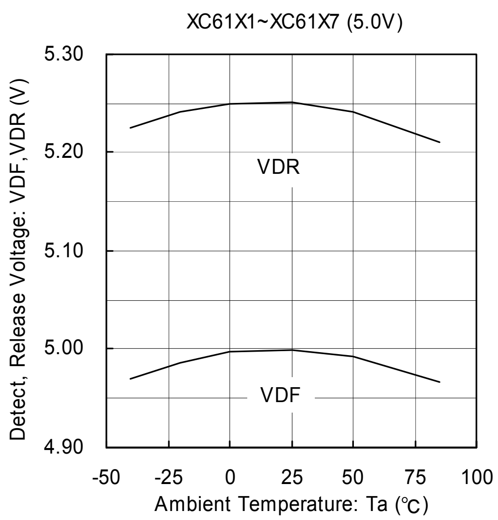
(1.2) Supply Current vs. Input Voltage (Continued)




(2) Detect, Release Voltage vs. Ambient Temperature



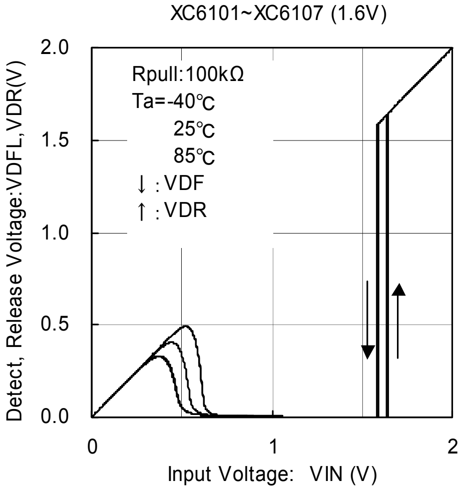



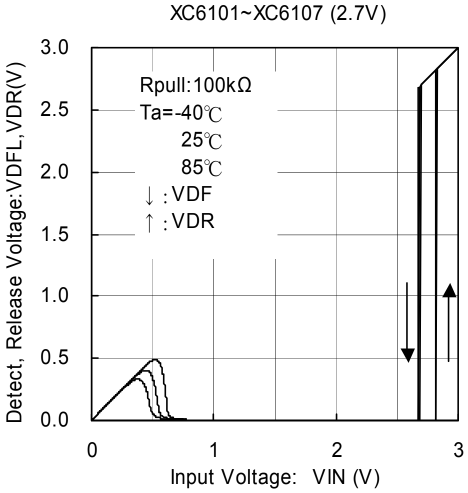



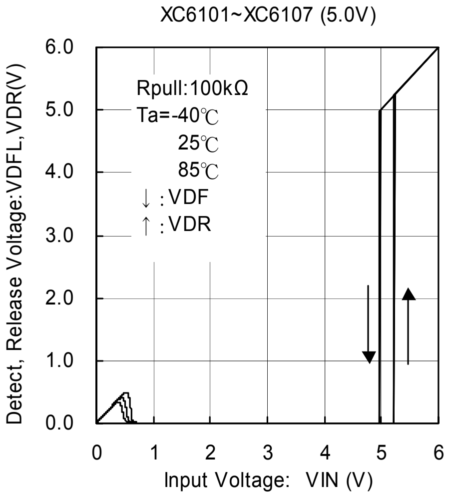

* ‘X’ represents both ‘0’ and ‘1’. (ex. XC61X1⇒XC6101 and XC6111)

# ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

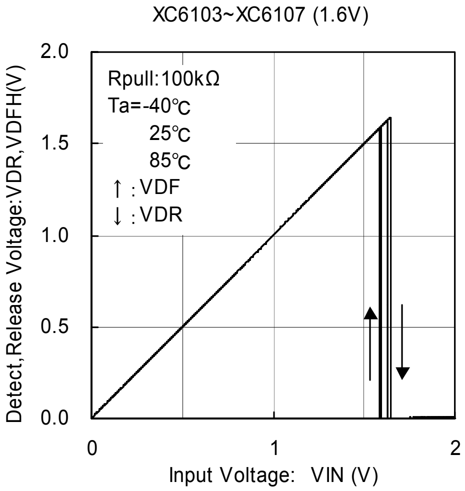
(3.1) Detect, Release Voltage vs. Input Voltage (VDFL)

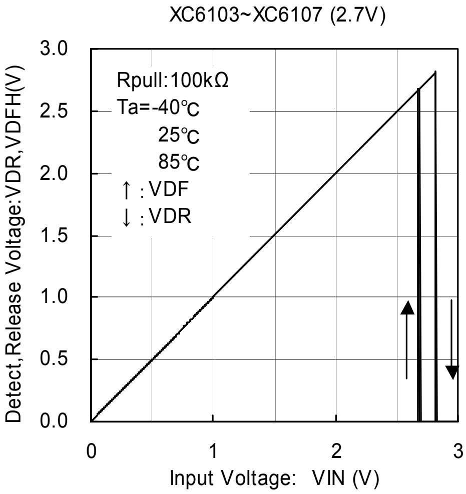



(3.2) Detect, Release Voltage vs. Input Voltage (VDFH)

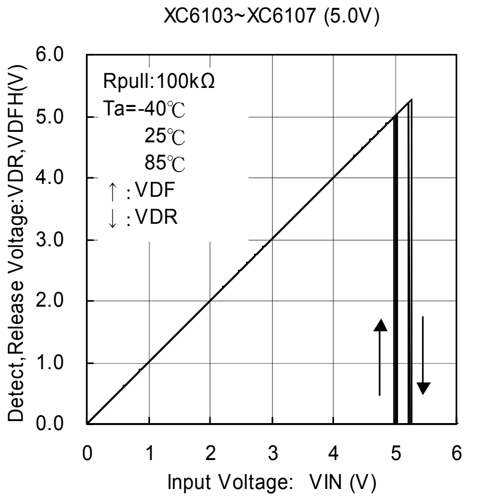


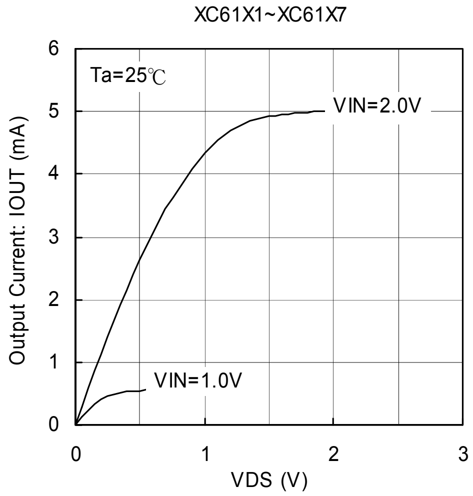

* 'X' represents both '0' and '1'. (ex. XC61X1⇒XC6101 and XC6111)

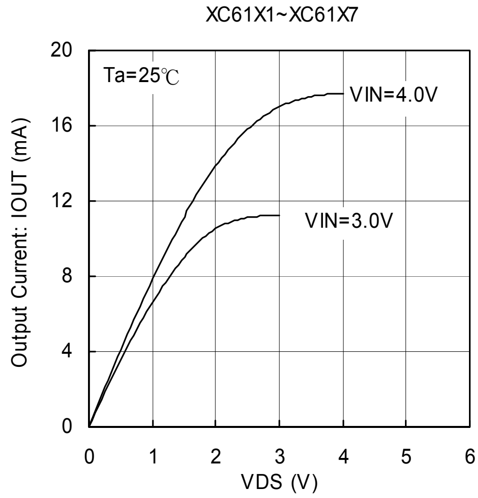
## ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(3.2) Detect, Release Voltage vs. Input Voltage ($V_{DFH}$) (Continued)

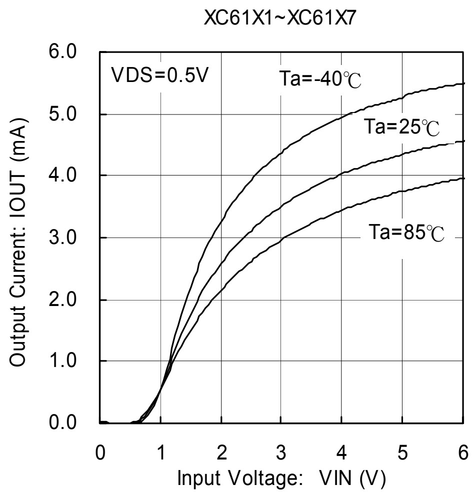



(4) N-ch Driver Output Current vs. $V_{DS}$



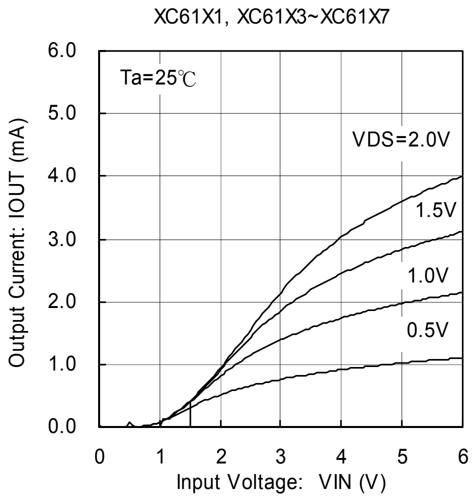

(5) N-ch Driver Output Current vs. Input Voltage



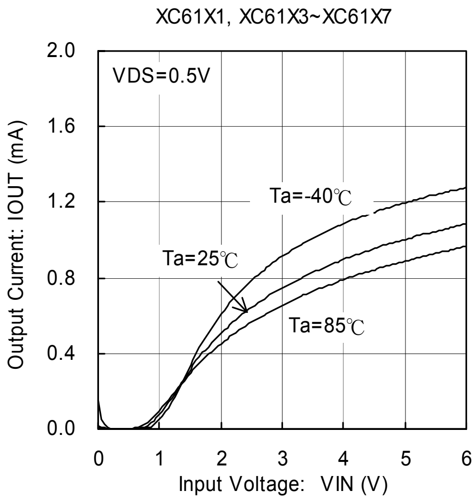

* ‘X’ represents both ‘0’ and ‘1’. (ex. XC61X1⇒XC6101 and XC6111)

## ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

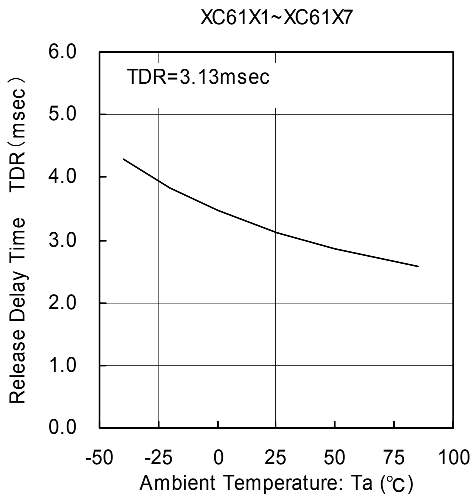
(6) P-ch Driver Output Current vs. Input Voltage 1

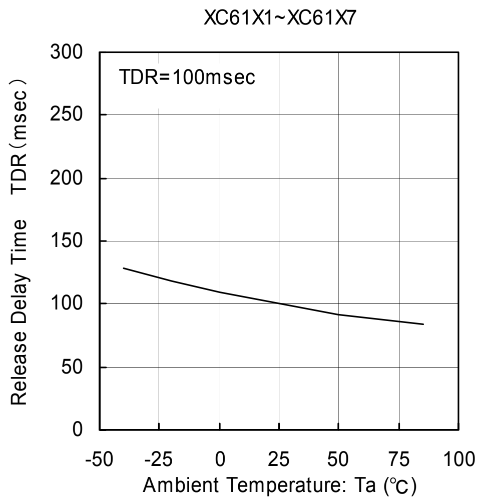


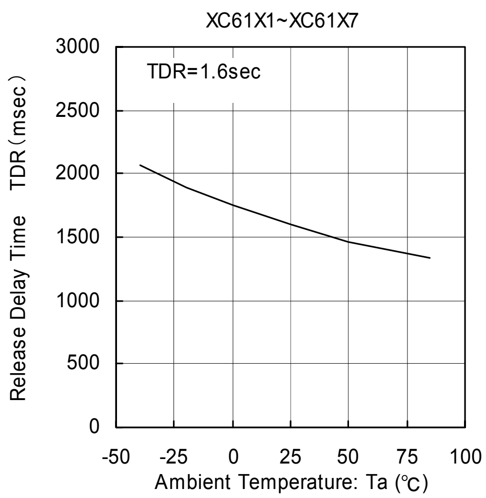

(7) P-ch Driver Output Current vs. Input Voltage 2




(8) Release Delay Time vs. Ambient Temperature



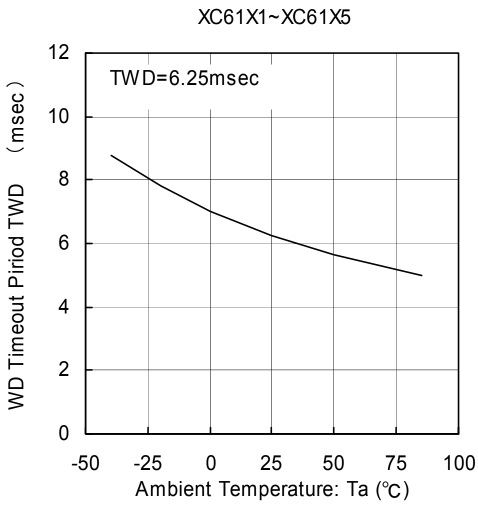



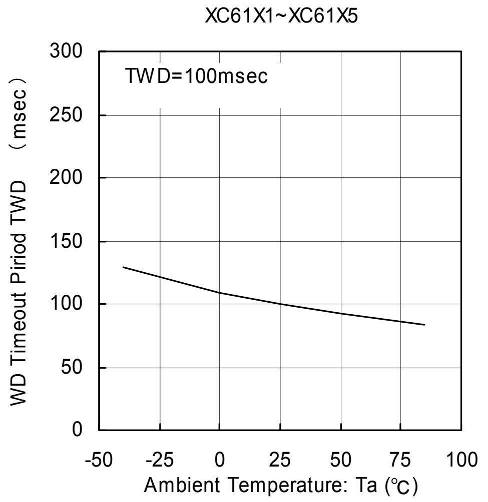



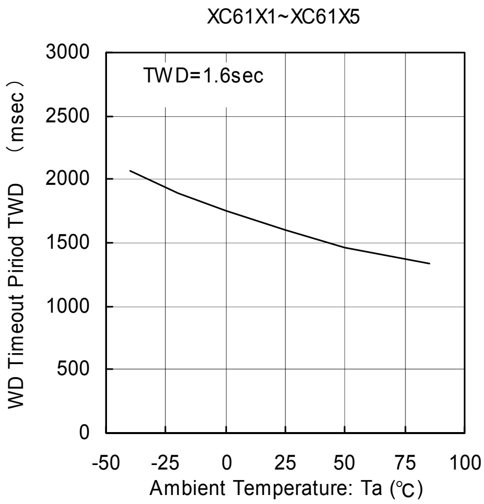

* ‘X’ represents both ‘0’ and ‘1’. (ex. XC61X1⇒XC6101 and XC6111)

## ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

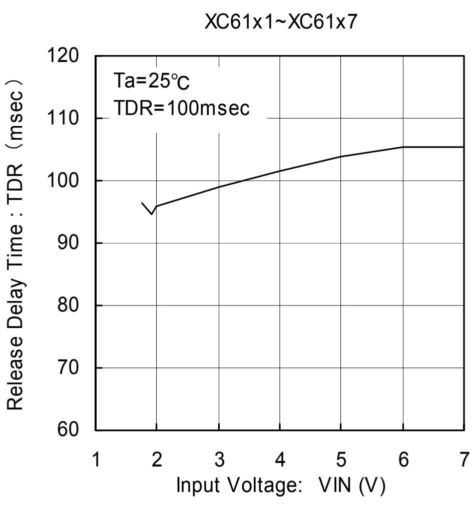
(9) Watchdog Timeout Period vs. Ambient Temperature



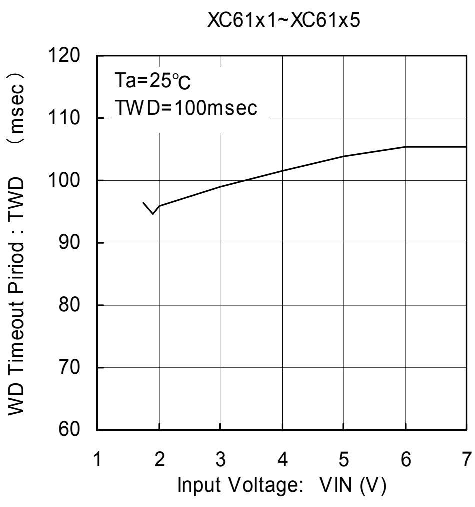




(10) Release Delay Time vs. Input Voltage



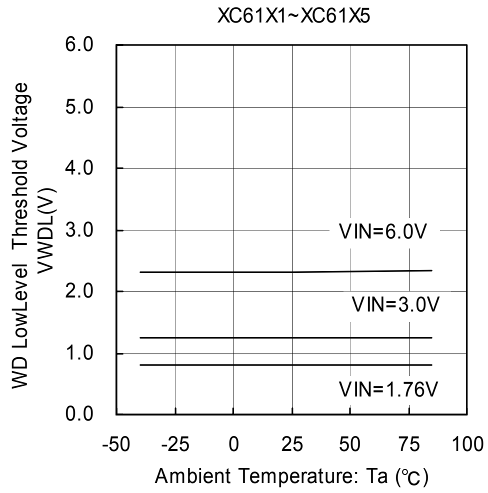

(11) Watchdog Timeout Period vs. Input Voltage



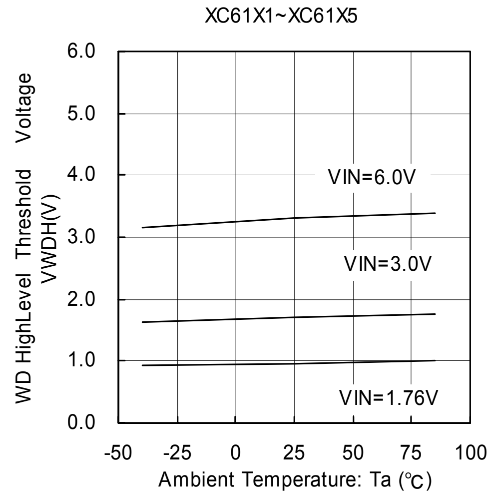

* ‘X’ represents both ‘0’ and ‘1’. (ex. XC61X1⇒XC6101 and XC6111)

## ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

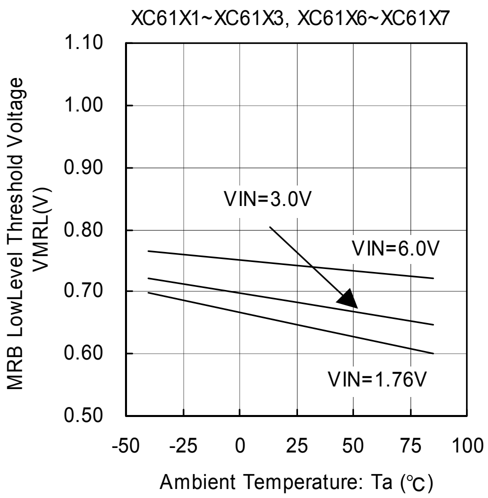
(12) Watchdog Low Level Voltage vs. Ambient Temperature



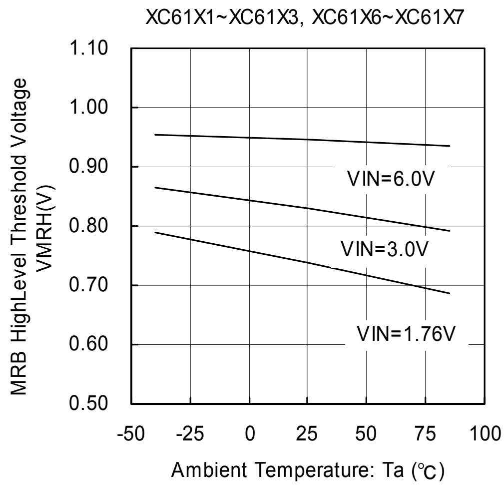

(13) Watchdog High Level Voltage vs. Ambient Temperature




(14) MRB Low Level Voltage vs. Ambient Temperature




(15) MRB High Level Voltage vs. Ambient Temperature




* ‘X’ represents both ‘0’ and ‘1’. (ex. XC61X1⇒XC6101 and XC6111)

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